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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,913	10/21/2003	Toshihide Suzuki	1614.1370	3762

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EXAMINER	
JONES, PRENELL P	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

10

Office Action Summary	Application No.	Applicant(s)	
	10/688,913	SUZUKI, TOSHIHIDE	
	Examiner	Art Unit	
	Prenell P. Jones	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-10* is/are rejected.

7)☐ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 5-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiramizu et al (US PG PUB 20040151506) in view of Mori et al (US Pat 4,727,541).

Regarding claim 1 and 8, Shiramizu et al (US PG PUB 20040151506) discloses a receiver and transmitter circuits that communicate with optical signals/data signals and clock signals via optical fiber communication paths (Abstract), wherein the transmitter circuit includes multiplexing, clock control circuit (paragraph 0063, 0064, 0074), modulation and amplification circuits, multiple clocks, multiple data signals are multiplexed and synchronized based on clock signal, plurality of multiplexer connected at the timing of respective clock signals (Figs. 2-5, paragraphs 0029, 002, 0053, 0068, 0080-0085), whereby the multiplexing circuit includes a selector (38) and multiple clocks, wherein the selector multiplexes multiple data signal inputs (paragraph 0092-0094), and transmitter circuit includes a multiplier which includes a 90 degree phase shifter is inputted to an EXOR circuit., and a control clock (28a) generating a first/second CLK 90 degrees phase shift (Figs. 5 and 6, paragraph 0074). However, Shiramizu is silent on a second selector multiplexing data with respect to a second clock.

In a data transmission system, Mori et al (US Pat 4,727,541) discloses a utilizing optical data transmission, wherein the architecture includes plurality multiplexers (MUX1 and MUX2),

plurality of selectors (SEL1 and SEL2), plurality de-multiplexers (DMUX1 and DMUX2), and EXOR gates for synchronization (col. 3, line 15-55, Fig. 7, col. 10, line 35-67, col. 12, line 50-55), wherein SEL1 and SEL2 are both indirectly coupled to both MUX1 and MUX2, therefore, each MUX consist of two selectors (SEL1 and SEL2)/first selector and second selector, data trains/data signals are multiplexed (col. 5, line 4 thru col. 6, line 68), multiple clocks (col. 9, line 1 thru col. 10, line 57), wherein multiplexed data trains are synchronized with respect to a reference clock.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a second selector of a multiplexing circuit that synchronize multiplexing data with respect to a second clock as taught by Mori with the teachings of Shiramizu for the purpose of further enhancing the operation frequency of a synchronous digital circuit as it is associated in a receiver and transmission circuit.

Regarding claim 2, 5 and 9, as indicated above, Shiramizu discloses a receiver and transmitter circuits that communicate with optical signals/data signals and clock signals via optical fiber communication paths (Abstract), wherein the transmitter circuit includes multiplexing, clock control circuit (paragraph 0063, 0064, 0074), modulation and amplification circuits, multiple clocks, multiple data signals are multiplexed and synchronized based on clock signal, plurality of multiplexer connected at the timing of respective clock signals (Figs. 2-5, paragraphs 0029, 002, 0053, 0068, 0080-0085), whereby the multiplexing circuit includes a selector (38) and multiple clocks (CLK1, CLK2, RefCLK), wherein the selector multiplexes multiple data signal inputs (paragraph 0092-0094), and transmitter circuit includes a multiplier which includes a 90 degree phase shifter is inputted to an EXOR circuit., and a control clock (28a) generating a first/second CLK 90 degrees phase shift (Figs. 5 and 6, paragraph 0074).

Shiramizu further discloses clock signals (CLK1, CL2) synchronized with a reference clock (RefCLK), wherein the RefCLK is a third clock signal (paragraph 0063).

Regarding claim 3 and 10, Shiramizu further discloses that the clock signals (CLK1, CLK2) can possibly maintain a clock signal having a frequency f1/2 the RefCLK/third clock (paragraph 0080, 0082).

Regarding claim 6 and 7, Shiramizu et al (US PG PUB 20040151506) discloses a receiver and transmitter circuits that communicate with optical signals/data signals and clock signals via optical fiber communication paths (Abstract), wherein the transmitter circuit includes multiplexing, clock control circuit (paragraph 0063, 0064, 0074), modulation and amplification circuits, multiple clocks, multiple data signals are multiplexed and synchronized based on clock signal, plurality of multiplexer connected at the timing of respective clock signals (Figs. 2-5, paragraphs 0029, 002, 0053, 0068, 0080-0085), whereby the multiplexing circuit includes a selector (38) and multiple clocks, wherein the selector multiplexes multiple data signal inputs (paragraph 0092-0094), and transmitter circuit includes a multiplier which includes a 90 degree phase shifter is inputted to an EXOR circuit., and a control clock (28a) generating a first/second CLK 90 degrees phase shift (Figs. 5 and 6, paragraph 0074). Shiramizu further discloses phase shifters 51 and 51a (changing timing/timing adjustment circuit) (paragraph 0031, 0102, 0107). However, Shiramizu is silent on a second selector multiplexing data with respect to a second clock and a second timing adjustment circuit.

In a data transmission system, Mori et al (US Pat 4,727,541) discloses a utilizing optical data transmission, wherein the architecture includes plurality multiplexers (MUX1 and MUX2), plurality of selectors (SEL1 and SEL2), plurality de-multiplexers (DMUX1 and DMUX2), and

EXOR gates for synchronization (col. 3, line 15-55, Fig. 7, col. 10, line 35-67, col. 12, line 50-55), wherein SEL1 and SEL2 are both indirectly coupled to both MUX1 and MUX2, therefore, each MUX consist of two selectors (SEL1 and SEL2)/first selector and second selector, data trains/data signals are multiplexed (col. 5, line 4 thru col. 6, line 68), multiple clocks (col. 9, line 1 thru col. 10, line 57), wherein multiplexed data trains are synchronized with respect to a reference clock.

Mori further discloses multiple shift clock generators/delay elements for adjusting the phase of a clock (Fig. 11, col. 11, line 65 thru col. 12, line 25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a second selector of a multiplexing circuit that synchronize multiplexing along with a second timing adjustment circuit data with respect to a second clock as taught by Mori with the teachings of Shiramizu for the purpose of further enhancing the operation frequency of a synchronous digital circuit as it is associated in a receiver and transmission circuit.

Allowable Subject Matter

3. Claims 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The combined prior art of Shiramizu et al (US PG PUB 20040151506) and Mori et al (US Pat 4,727,541) who discloses a receiver and transmitter circuits that communicate with optical signals/data signals and clock signals via optical fiber communication paths, wherein the transmitter circuit includes multiplexing, clock control circuit, phase shifter, modulation and

amplification circuits, multiple clocks, multiple data signals are multiplexed and synchronized based on clock signal, plurality of multiplexer connected at the timing of respective clock signals, whereby the multiplexing circuit includes a selector (38) and multiple clocks, wherein the selector multiplexes multiple data signal inputs, and transmitter circuit includes a multiplier which includes a 90 degree phase shifter is inputted to an EXOR circuit., and a control clock (28a) generating a first/second C:LK 90 degrees phase shift, and a second selector multiplexing data with respect to a second clock, utilizing optical data transmission, wherein the architecture includes plurality multiplexers (MUX1 and MUX2), plurality of selectors (SEL1 and SEL2) and clock signals (CLK1 and CLK2) are synchronized with respect to a reference clock.

The prior art fails to teach or suggest fairly with respect to claim 4, a second latch circuit which receives a third clock signal as a reversed clock input, and receives an output of said first latch circuits as data input, wherein an inverse of an output of a second latch circuit is input into a first latch circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones

May 9, 2007

CHI PHAM
SUPERVISORY PATENT EXAMINER

5/14/07